A1
require converting the 188-byte packet of the transport stream into 32-bit or 64-bit wide words of information and transporting the words to memory or the video adapter across the PCI bus.

Please replace the paragraph beginning at page 2, line 20 with the following rewritten paragraph:

A2
In order to provide data to the video adapter of the prior art, it is necessary for separate printed circuit boards to be used to implement the transport stream converter and video adapter. Separate boards allow a PCI interface to the video memory associated with the video adapter. Separate board increase overall system costs. In addition to increasing overall system costs, the data stream requires approximately 5 Mbytes of PCI bandwidth, thereby limiting the bandwidth available to other system resources. In addition, when analog video is received and digitized (not illustrated), by the prior art system the PCI band data bandwidth is approximately 25 Mbytes.

Please replace the paragraph beginning at page 2, line 28 with the following rewritten paragraph:

A3
Another proposed method for receiving DVB data was to use the side port of a video graphics adapter in order to receive the transport stream information. However, the video side port is designed to only receive uncompressed digital video instead of compressed MPEG transport stream. A format conversion chip is needed between the DVB demodulator output and video side port to convert a transport stream into a compatible ITU-656 ancillary stream (digital video or data format) like format. This will add cost to system implementation. Another problem is that the data in the transport stream is not fully compliant with ITU-656 data. (Values such as 00 and FF are not allowed in an ITU-656 stream but allowed in a transport stream. So this implementation cannot work if the video side port is strictly designed for ITU-656 data streams.)

Please replace the paragraph beginning at page 4, line 5 with the following rewritten paragraph:

A4
A method and apparatus for receiving one of a compressed video stream and an uncompressed video stream is disclosed. The uncompressed video stream may be ZOOM

VIDEO data or a digitized analog video signal. The compressed video stream may be an MPEG TRANSPORT STREAM data from a High Definition Television (HDTV) broadcast. A video graphics adapter is configured to properly receive one of the two types of video data. The received data and control signals are monitored to provide a second set of control signals that are used by a packer, a window controller, and an address generator. The packer packs data into a format which is compatible with the frame buffer memory. The window controller controls the amount of data written into frame buffer memory. The address generator generates proper frame buffer addresses for the data. The data is stored within a pre-defined area of graphics memory such as a frame buffer. The data can be transferred to system memory when a buffer is full.

A4

Please replace the paragraph beginning at page 4, line 16 with the following rewritten paragraph:

Figure 2 illustrates a system in accordance with the present invention. A digital video broadcast (DVB) signal is received by the tuner 210. The tuner 210 provides a representation of the received analog signal to the demodulator 220. The demodulator 220 demodulates the signal to provide a digital TRANSPORT STREAM to one or both of the transport demultiplexor 240 and the video adapter 230. In accordance with the present invention, the video adapter 230 receives the TRANSPORT STREAM and buffers it into a video memory, or frame buffer. Upon filling the frame buffer, the TRANSPORT STREAM data is either further utilized by the video adapter 230, or at least partially provided to system components, such as the Central Processing Unit (CPU) 250, or the memory 260. A second data path receives an analog signal, such as would normally be associated with television broadcasts, at tuner 211. The signal from tuner 211 is provided to a NTSC/PAL/SECAM demodulator 221 to provide a digital representation of the received analog signal. Note that the tuner 211 and demodulator 221 may be the same, or different, from the tuner 210 and demodulator 220.

A5

Please replace the paragraph beginning at page 5, line 1 with the following rewritten paragraph:

A6

Figure 3 illustrates the video adapter 230 in greater detail. In normal operation, the video adapter 230 processes video and/or graphics information and provides a signal labeled VIDEO OUT. The VIDEO OUT signal is used to drive an image onto an external display device (not

A6

shown). In accordance with the present invention, the video adapter 230 includes a capture block 310 to receive a data stream, a graphics engine 320, a graphics memory 330, and a PCI interface 340.

Please replace the paragraph beginning at page 5, line 10 with the following rewritten paragraph:

A7

In operation, the digital data stream, such as the TRANSPORT STREAM from the demodulator 220 of Figure 2, is received at the capture block 310. Where the digital data stream is a TRANSPORT STREAM, the TRANSPORT STREAM comprises both data and control information. Generally, the TRANSPORT STREAM includes a plurality of packets. Each packet of TRANSPORT STREAM information includes a synchronization byte followed by a predetermined number of data bytes. The data bytes can include routing information stored as header information, or as raw data as identified by the header information. When the data is transmitted as header information, it is in an uncompressed form that indicates the type of data that is to follow the header. A single header can be included in one or more packets.

Please replace the paragraph beginning at page 5, line 16 with the following rewritten paragraph:

A8

The capture block 310 receives the TRANSPORT STREAM information and provides the necessary data and control in order to store the compressed TRANSPORT STREAM data within the graphics memory 330. The memory 330 is accessed over the bus 350. In a specific embodiment, the memory 330 is a frame buffer used by the graphics engine 320. The memory 330 is connected to the capture block 310 through the bus 350 which accommodates the necessary data, address, and control lines for accessing memory 330. The graphics memory 330 is also connected to the graphics engine 320 and the PCI Interface 340 through the bus 350.

Please replace the paragraph beginning at page 5, line 23 with the following rewritten paragraph:

A9

In accordance with the present invention, the graphics memory 330 can operate as a frame buffer for the graphics engine 320, or as a buffer to store the TRANSPORT STREAM data. The PCI Interface 340 provides an interface between the internal bus 350 to an external

PCI bus. Generally, the PCI Bus will be a system bus. It should be noted that while a PCI interface 340 has been shown, the present invention anticipates the use of other type bus interfaces. Therefore, the PCI interface 340 may be any bus type whether an industry standard or a proprietary interface.

A9

Please replace the paragraph beginning at page 6, line 1 with the following rewritten paragraph:

Figure 4 illustrates the capture block 310 in greater detail. Specifically, the capture block 310 is shown to receive a number of different types of video data. As indicated, 8-bit DVS (Digital Video Stream) video and ZOOM VIDEO is received. Generally, the 8-bit DVS and ZOOM VIDEO data are ITU-601 or ITU-656 related digital video streams. These streams are not compressed video streams. However, the HDTV TRANSPORT STREAM received by the capture block 310 of Figure 4, as previously mentioned, is a compressed video stream, such as MPEG 2. While the DVS, ZOOM VIDEO and TRANSPORT STREAM are illustrated in Figure 4 separately, in operation, the signals will share inputs that can be multiplexed, or de-multiplexed as needed. For example, the data bits from each format can be received by a common set of pins

A10

Please replace the paragraph beginning at page 6, line 10 with the following rewritten paragraph:

A signal labeled VIDEO SELECT is used to indicate to the Capture Block 310, which type of video is to be received. By allowing for one of a plurality of types of digital video data to be received, greater flexibility is realized within the Video Graphics Adapter (VGA). This reuse of common circuitry allows for an efficient implementation of the present invention. Yet another advantage of the system as illustrated in Figure 3 is that it reduces system costs over the prior art in that the PCI interface 340 already residing within the VGA is used to store transport buffered stream data.

A11

Please replace the paragraph beginning at page 6, line 20 with the following rewritten paragraph:

A12

In Figure 5, the TRANSPORT STREAM, and any other type of digital video, such as ZOOM VIDEO, is received by the video-in controller 510 of Figure 5. The TRANSPORT

A12

STREAM includes the signals 501, which include a multi-bit data signal (DATA), a synchronization signal (SYNCH), a data valid signal (DVALID), and a clock signal (TCK). The ZOOM VIDEO data is illustrated as a bus. However, it should be noted, that the signals 501 can be multiplexed and/or de-multiplexed (not shown) to receive either ZOOM VIDEO or TRANSPORT STREAM data.

Please replace the paragraph beginning at page 6, line 27 with the following rewritten paragraph:

Sub C1 A13

The video-in controller 510 acts as a stream interface control to convert the received signal, whether ZOOM VIDEO or a TRANSPORT STREAM, into a Start of Field (SOF) signal, a Start of Active (SOA) signal, an End of Active (EOA) signal, a Data Active (DACTIVE) signal, and a Video Data (VDATA) signal. For ZOOM video, these signals are represented in Figures 6 and 7.

Please replace the paragraph beginning at page 7, line 3 with the following rewritten paragraph:

Sub C2 A14

Figure 6 represents a frame of video 610. In a specific embodiment, the video is representative of ZOOM VIDEO. The frame of video 610 has a Vertical Blanking Interval (VBI) which resides in the first few lines of video. The VBI information is not displayed, but can be used to provide data for other operations of functions. Following the VBI portion, VIDEO is provided. Within the VIDEO portion, an active video 620 is illustrated which represents a portion of the VIDEO to actually be displayed. At the beginning of each line of the frame 610, a Start of Active (SOA) pulse is provided. At the end of each line of the frame 610, an End of Active (EOA) video signal is provided. At the beginning the first line of the frame 610, the start of a new frame is indicated by a Start of Frame (SOF) indicator. Note that the SOA and EOA refers to the entire VIDEO portion relative to the transmitted data. The active video 620 is the active video relative to the user.

Please replace the paragraph beginning at page 7, line 15 with the following rewritten paragraph:

The active video620 of Figure 6 indicates the portion of the received VIDEO to be displayed. One example of the active video620 varying from the received VIDEO is when the received video to be displayed on a standard television is High Definition Television (HDTV), which has a different aspect ratio than standard television. In this mode of operation, it is desirable to select only a portion of the HDTV frame for display on a standard television screen. In order to specify the desired active video 620, it is necessary to specify a Y OFFSET indicated where the first line of active video 620 begins, a X OFFSET indicating which pixel is the first pixel of active video 620, a WIDTH indicating the number of pixels in a containing active video 620, and a HEIGHT indicating the number of lines containing the active video. Note that the X OFFSET, and Y OFFSET are illustrated to be relative to the first line and pixel of the frame 610. However, in other embodiments, other reference locations can be indicated.

A15

Please replace the paragraph beginning at page 7, line 26 with the following rewritten paragraph:

A16

Figure 7 illustrates the signals associated with ZOOM VIDEO. The ZOOM VIDEO signals received by the video-in controller 510 are substantially similar to the signals provided by the video-in controller 510, except that no DACTIVE signal is received. Therefore, since there is no equivalent signal to DACTIVE in ZOOM VIDEO, the DACTIVE signal from video-in controller 510 specified is asserted when the video-in controller 510 receives data.

Please replace the paragraph beginning at page 8, line 3 with the following rewritten paragraph:

Sub C3

A17

In operation, the window controller 520 receives the SOF, SOA, and EOA signals from the video-in controller 510. In addition, the window controller 560 receives, and/or has access to values indicating the X OFFSET, Y OFFSET, WIDTH, and HEIGHT values associated with Figure 6. These values can be provide in any number of manners, including inputs to the window controller 520, or by accessing register locations. From the received values and signals, the window controller 520 generates a second set of control signals: Window control Start of

A17

Field (WSOF); Window control End of Field (WEOF); Window control End of Line (WEOL); Vertical Active (VACTIVE); and Horizontal Active (HACTIVE). These signals are further described with reference to the table below, and the relationship of the signal WSOF, WEOF, and WEOL are illustrated in Figure 8.

Please replace the paragraph beginning at page 8, line 14 with the following rewritten paragraph:

A18

WINDOW CONTROL OPERATION FOR ZOOM VIDEO

SIGNAL	DESCRIPTION
WSOF	Pulse active when at first pixel of active video.
WEOF	Pulse active at last pixel of active video.
WEOL	Pulse active at end of each line of active video.
HACTIVE	Asserted when pixel count within WIDTH.
VACTIVE	Asserted when line count is with in HEIGHT.

Please replace the paragraph beginning at page 8, line 24 with the following rewritten paragraph:

A19

The signal WSOF (Window control Start of Field) provides an asserted pulse when the first pixel of the active video 620 is encountered. The first pixel location can be determined by comparing the X OFFSET and Y OFFSET values to the current pixel and line numbers, which are maintained by the system. For example, in one implementation, the Y OFFSET represents the first line of active video 620, while the X OFFSET represents the first pixel of active video 620 within a line. This is represented in Figure 8, where the signal WSOF is active at the same time as the clock pulse labeled L. The clock pulse L represents the time at which the first pixel of the active video 620 is available.

Please replace the paragraph beginning at page 9, line 3 with the following rewritten paragraph:

The signal WEOF provides an asserted pulse when the last pixel of the active video 620 is encountered. The last pixel location can be determined by comparing the sum of the WIDTH and X OFFSET values to the current pixel number, and comparing the sum of the HEIGHT and the Y OFFSET values to the line number. For example, in one implementation, the X OFFSET plus the WIDTH less one indicates the last bit of active video 620 associated with a line. Likewise, Y OFFSET plus the HEIGHT less one indicates the last line of active video 620. Therefore, by monitoring these values, the WEOF signal can provide an asserted pulse when both the last line and pixel of an active video 620 region is encountered. This is illustrated in Figure 8, where the signal WEOF is active at a time in conjunction with the clock pulse labeled N. The clock pulse N represents the time at which the last pixel of the active video 620 is available.

A20

Please replace the paragraph beginning at page 9, line 14 with the following rewritten paragraph:

The signal WEOL provides an asserted pulse when the last pixel of a line of active video 620 is encountered. The last pixel of a line can be determined by comparing the sum of the WIDTH and X OFFSET values to the current pixel number. For example, in one implementation, the X OFFSET plus the WIDTH minus one represents the last bit of a line of active video 620. This number can be compared to the current pixel number to determine whether the end of line has occurred. WEOL is represented in Figure 8, where the signal WEOL is active at a time in conjunction with the clock pulses labeled M and N. The clock pulses M and N represents the time at which the last pixel of a line of data is available.

A21

Please replace the paragraph beginning at page 9, line 22 with the following rewritten paragraph:

The signal HACTIVE is asserted when the current pixel location is within the WIDTH region. Note that a pixel does not have to be in the active video 620 in order for HACTIVE to be asserted. This allows for an embodiment whereby only the pixel number is monitored and

A22

A22

compared to the values associated with the WIDTH of the active video 620. Likewise, the VACTIVE signal is asserted when the current line number is within the HEIGHT region indicated in Figure 6.

Please replace the paragraph beginning at page 9, line 28 with the following rewritten paragraph:

A23

It will be understood by one skilled in the art, that the exact time at which the window controller 520 provides a given control signal can vary depending upon specific embodiments. For example, the WEOL signal can be asserted in conjunction with the last pixel, or after the last pixel.

Please replace the paragraph beginning at page 10, line 4 with the following rewritten paragraph:

A24

Referring to Figure 5, the signals generated by the window controller 520 are used by the packer 540 and the address generator 530 to provide data and addresses to the buffer. In one embodiment, the packer 640 receives 8-bit bytes of data, and combines them to form larger data words labeled VIDEO DATA. For example, the VIDEO DATA signal can comprise 32, 64, or 128 bit words of video data. The width of VIDEO DATA can be fixed or programmable. The DACTIVE, HACTIVE, and VACTIVE signals qualify the VDATA received by the packer 540.

Please replace the paragraph beginning at page 10, line 9 with the following rewritten paragraph:

A25

For ZOOM VIDEO, DACTIVE is always asserted. Therefore, the packer 540 uses the HACTIVE and VACTIVE data to qualify VDATA. For example, when both HACTIVE and VACTIVE are asserted, the data value received on VDATA is within the active video 620, and will be included by the packer 540 within the VIDEO DATA. If either of HACTIVE and VACTIVE are inactive, the data value received on VDATA is not within the active video, and will not be included by the packer 540 as part of the VIDEO DATA.

Please replace the paragraph beginning at page 10, line 15 with the following rewritten paragraph:

The described embodiment for receiving ZOOM VIDEO provides for an efficient means to receive only a desired portion of VIDEO DATA, however, the data received needs be readily associated with a specific line and a pixel in order to determine where the active video resides. In contrast, DVB data is compressed, and visibility as to the line and pixel locations not readily available without decompression of the data first occurring. In specific embodiments, it is desirable to perform such decompression of the data first occurring. In specific embodiments, it is desirable to perform such decompression by other parts of the system, or at least to store the compressed data in other parts of the system. Therefore, one embodiment of the present invention further allows compressed data, such as DVB TRANSPORT STEAM data, to be buffered within the graphics memory 330 of Figure 3.

A26

Please replace the paragraph beginning at page 10, line 25 with the following rewritten paragraph:

Figure 9 illustrates a timing diagram representing signals associated with the TRANSPORT STREAM of Figure 2. The TRANSPORT STREAM includes a signal labeled TCK, which provides one clock pulse to qualify each byte of data. A synchronization (SYNCH) signal indicates the beginning of a new line or packet of information. In addition, a data valid signal (DVALID) indicates when the packet data being transmitted is valid.

A27

Please replace the paragraph beginning at page 11, line 3 with the following rewritten paragraph:

In response to the TRANSPORT STREAM, the video-in controller 520 drives the signals SOF, SOA, EOA, DACTIVE and VDATA. The manner in which these signals are generated is different for a TRANSPORT STREAM than for the ZOOM VIDEO previously discussed. The table below indicates the operation of the window controller 520 for TRANSPORT STREAM reception.

A28

Please replace the paragraph beginning at page 11, line 9 with the following rewritten paragraph:

A29

OPERATION FOR RECEPTION OF A TRANSPORT STREAM

VIDEO-IN SIGNAL	DESCRIPTION
SOF	Pulse active to indicate the first byte of a TRANSPORT STREAM packet to be stored in buffer.
SOA	Pulse active to indicate the first byte of a TRANSPORT STREAM packet.
EOA	Pulse active to indicate the last byte of a TRANSPORT STREAM packet.
DACTIVE	Asserted to indicate invalid bytes as indicated by DVALID.
VDATA	Data from TRANSPORT STREAM.

Please replace the paragraph beginning at page 11, line 20 with the following rewritten paragraph:

A30

During reception of the TRANSPORT STREAM, the SOF signal provides an asserted pulse to indicate that the first byte to be stored in the graphics memory 330 is present. In one embodiment, the video-in controller 510 will use a counter to keep track of the number of lines and bytes of compressed data provided to the window controller 520. When the number of lines sent to the window controller 520 exceeds the number of lines available in the graphics memory 330, the SOF is pulsed again to indicate a new first byte to be stored in the graphics memory. The SOF signal of Figure 9 illustrates two pulses. The first pulse corresponds to TCK 1, which is associated with the first data byte to be stored in the graphics memory 330. The second SOF pulse occurs on the first TCK after line N has been transmitted, where N is the total number of lines to be stored in the graphics memory 330. Note that in Figure 9, the number of bytes in a line of video memory is 138. Coincidentally, this is the same number of bytes that are in a

A30 TRANSPORT STREAM packet. In other embodiments, the line size is different than the packet size, such that a line of video memory will not necessarily contain an integer number of packets.

Please replace the paragraph beginning at page 12, line 5 with the following rewritten paragraph:

A31 Note that the graphics memory 330 can have one or more buffer locations. Where multiple buffer locations are present, it is possible to switch between buffers when one buffer is full, and continue storing data without delay, or with minimal delay, in a second buffer. If only one frame buffer is available, and it becomes full, it will be necessary to write at least some of the graphics memory 330 contents to system memory, or lose data by writing over the stored values. By using a dual ported graphics memory 330, it would be possible to buffer data and transmit it to the system simultaneously. In another embodiment, a single ported memory can also do the job, by interleaving between read and write operations.

Please replace the paragraph beginning at page 12, line 13 with the following rewritten paragraph:

A32 The video-in controller 510 signal SOA indicates that the first byte of a TRANSPORT STREAM packet is being transported. The SOA signal can be qualified by the TRANSPORT STREAM's SYNCH signal. There are three such SOA pulsed indicated in Figure 9.

Please replace the paragraph beginning at page 12, line 24 with the following rewritten paragraph:

A33 The signal DACTIVE indicates when the data presented to the packer 540 is valid. As indicated in Figure 9, the signal DACTIVE will generally mirror the signal DVALID of the TRANSPORT STREAM.

Please replace the paragraph beginning at page 13, line 1 with the following rewritten paragraph:

A34 The window controller 520 receives the SOF, SOA, and EOA signals from the video-in controller 510 representing the TRANSPORT STREAM. In addition, the window controller 520 receives, and/or has access to, values indicating the X OFFSET, Y OFFSET, WIDTH, and

HEIGHT values associated with Figure 6. For TRANSPORT STREAM reception, the X OFFSET and Y OFFSET will generally be zero, the WIDTH will be number of bytes in the TRANSPORT STREAM, and the HEIGHT will indicate the number of lines to be stored in the graphics memory 330. From the received values and signals, the window controller 520 generates the signals: Window control Start of Field (WSOF); Window control End of Field (WEOF); Window control End of Line (WEOL); Vertical Active (VACTIVE); and Horizontal Active (HACTIVE). These signals are further described with reference to the table below.

A34

Please replace the paragraph beginning at page 13, line 11 with the following rewritten paragraph:

WINDOW CONTROL OPERATION FOR TRANSPORT STREAM DATA

A35

SIGNAL	DESCRIPTION
WSOF	Pulse qualified to SYNCH signal and counter.
WEOL	Pulse qualified to EOA.
WEOF	Pulse qualified to SOF and EOA.
HACTIVE	Assertion qualified to SOA and EOA when pixel count within WIDTH.
VACTIVE	Asserted when between SOA pulse and EOA pulse
HACTIVE	Asserted when between SOF pulse and WEOF.

Please replace the paragraph beginning at page 13, line 26 with the following rewritten paragraph:

A36

The signal WSOF signal provides an asserted pulse to indicate the first byte to be stored within a buffer of the graphics memory 330 buffer. For a specific embodiment, where the video-in controller 510 monitors and maintains the number of lines being written, the WSOF signal for a TRANSPORT STREAM will be analogous to the SOF signal generated by the video-in controller 510.

Please replace the paragraph beginning at page 14, line 3 with the following rewritten paragraph:

A37

The signal WEOF signal provides an asserted pulse to indicate the last byte to be stored in the current buffer location of the graphics memory 330. The window controller 520 generates the WEOF signal by comparing the number of EOA signal received since SOF was active, and comparing this number to the provided HEIGHT value. by setting the Y OFFSET to zero, and the HEIGHT value to the number of lines in the graphics memory 330, it is possible for the window controller 520 to generate the correct WEOF pulse without additional hardware.

Please replace the paragraph beginning at page 14, line 9 with the following rewritten paragraph:

A38

The signal HACTIVE is asserted when the current byte location is within the WIDTH region which is set to the number of bytes in a packet (188 bytes).

Please replace the paragraph beginning at page 14, line 11 with the following rewritten paragraph:

A39

The signal VACTIVE is asserted when the current data being received is to be stored in the current line of the buffer.

Please replace the paragraph beginning at page 14, line 13 with the following rewritten paragraph:

A40 Sub C4

The packer 540 provides a signal labeled ADDR GEN REQ, which indicates when a line of data is ready to be stored in the graphics memory 330. The graphics memory 330 address and control information, is provided to the graphics memory 330 by the address generator 630 when ADDR GEN REQ is active.

Please replace the paragraph beginning at page 14, line 25 with the following rewritten paragraph:

A41

An error signal can also be incorporated into the transport stream. When an error signal is received, a specific code can be generated and written with the data stream. Subsequent systems can be notified that an error occurred by monitoring the data and reacting accordingly.

Please replace the paragraph beginning at page 15, line 1 with the following rewritten paragraph:

A42

In this manner, compressed and uncompressed data can be stored in the frame buffer represented by graphics memory 330. Once an entire frame of data is stored in the graphics memory 330 the data can be written to system memory, or it can be decompressed by the graphics engine 320.

Please replace the paragraph beginning at page 15, line 5 with the following rewritten paragraph:

A43

By having the video-in controller 510 generate the SOF, SOA, EOA, DACTIVE, and VDATA in the manner indicated, it is possible to use much of the same hardware to implement a storage apparatus for both compressed and uncompressed video.

Please replace the paragraph beginning at page 15, line 8 with the following rewritten paragraph:

A44

Figure 11 illustrates a method in accordance with the present invention. Generally, the method of Figure 11 has been discussed with respect to the specific system herein. At step 1101, a determination is made whether a first or second type of video data is to be received. Specifically, the first type of data represents TRANSPORT STREAM data as indicated in step 1102. The second type of data represents a digital video stream different from a TRANSPORT STREAM, such as the ZOOM VIDEO signal discussed herein, as indicated at step 1103.

Please replace the paragraph beginning at page 15, line 14 with the following rewritten paragraph:

A45 At steps 1102 and 1103 the system is configured for either a TRANSPORT STREAM or a different digital video stream, respectively. As discussed with respect to TRANSPORT STREAM and ZOOM VIDEO herein, these configurations indicate how a video controller will generates its output signals.

Please replace the paragraph beginning at page 15, line 18 with the following rewritten paragraph:

A46 At step 1104, a secondary set of control signals is generated from the received data stream. This corresponds to the video-in controller 510 generating signals SOF, SOA, EOA, DACTIVE, AND VDATA, as discussed herein.

Please replace the paragraph beginning at page 15, line 21 with the following rewritten paragraph:

A47 At step 1105, at least a portion of the data stream is stored. Step 1105 corresponds to the window controller 520, packer 540, and address generator 530 working together as a data storage controller to store words of data in a buffer associated with graphics memory 330. These words of data will contain at least a portion of the data received by the video-in controller 510 in the manner discussed herein.

Please replace the paragraph beginning at page 15, line 26 with the following rewritten paragraph:

A48 At step 1106, the information stored in the graphics memory 330 is written to a system bus via the PCI interface of Figure 3.

Please replace the paragraph beginning at page 16, line 1 with the following rewritten paragraph:

Sub C A49 The present invention has been described with reference to specific embodiment. One of ordinary skill in the art will recognize that other embodiments may exist. For example, the data

storage described herein has been described with reference to using SOF/EOF/SOA/EOA video fields to store TRANSPORT STREAM data. In a similar manner, fields such as Start of VBI and End of VBI could be used to indicate when to store the transport stream data. Such an implementation would require the window controller 520 to provide indicators when VBI data is active and should be stored. By indicating the VBI data had the same number of lines of the buffer associated with the graphics memory 330, the TRANSPORT STREAM data can be stored.

A49 C5 cont

Please replace the paragraph beginning at page 16, line 9 with the following rewritten paragraph:

A50

Another variation would allow the TRANSPORT STREAM data to be stored in the buffer in a compressed form only when it is of a desired type of data. For example, the headers of the TRANSPORT STREAM can be monitored to allow only a specific type of data, such as video or audio, to be buffered.

Please replace the paragraph beginning at page 16, line 13 with the following rewritten paragraph:

A51

It should be further understood that specific functions and steps described may actually be implemented in hardware and/or in software. For example, the signal generation performed by the window controller 520 can be performed by a hardware engine, firmware such as in microcode executed on the processing engine or it may even be performed fully in software. In general, such functions can be performed in a processing module that may be a single processing device or a plurality of processing devices. Such a processing device may be a microprocessor, microcontroller, digital signal processor, microcomputer, portion of the central processing unit, state machine, logic circuitry, and/or any device that manipulates signals (e.g., analog or digital) based on operational instructions. The memory may be a single memory device or a plurality of memory devices. Such a memory device may be a read-only memory, random access memory, floppy disk memory, magnetic tape memory, erasable memory, portion of system memory, and/or any device that stores operational instructions in a digital format. Note that when the processing module implements one or more of its functions via a state machine or logic circuitry,

the memory storing the corresponding operational instructions is embedded within the circuitry comprising the state machine and/or logic circuitry.

Please replace the paragraph beginning at page 16, line 28 with the following rewritten paragraph:

The specific embodiments of the present invention disclosed herein are advantageous in that TRANSPORT STREAM data can be buffered in a portion of memory normally used by the video graphics adapter. Furthermore, the amount of overhead needed to store the TRANSPORT STREAM data is minimal because the system hardware/firmware/software is largely in place to handle the data. This is an advantage over other prior art embodiments which had dedicated hardware to merely convert TRANSPORT STREAM data into a useful format before be received by a VGA controller. By allowing transport stream data to be received directly by the VGA controller, cost savings and efficiencies are gained. In addition, variations of the specific embodiments are anticipated. For example, the uncompressed video may be digitized NTSC/PAL/SECAM signals as well.

Please replace the paragraph beginning at page 21, line 1 with the following rewritten paragraph:

A method and apparatus for storing a compressed video stream or an uncompressed video stream is disclosed. The uncompressed video stream may be ZOOM VIDEO data. The compressed video stream may be a TRANSPORT STREAM data from a High Definition Television (HDTV) broadcast. A video graphics adapter is configured to properly receive one of the two types of video data. The received data and control signals are monitored to provide a second set of control of data signal which are used by a packer and an window control to provide data of a predetermined width and control to an address generator. The data is buffered within a graphics memory such as a frame buffer. The graphics memory can be written to system memory when full, or accessed by the system memory controller during the fill operation if a multi-ported memory is used.